What is claimed is:

1. A semiconductor device test system comprising:

a plurality of comparator and driver units, each comparator and driver unit comprising a driver configured to drive an input signal pattern to be applied to one or more input pins of the semiconductor device and a comparator configured to compare data output from one or more output pins of the semiconductor device with a predetermined output signal pattern;

a plurality of control units, each control unit configured to electrically connect a corresponding comparator and driver unit to a pin of the semiconductor device in response to a control signal, wherein pins of the semiconductor device are divided into pin groups, each pin group having K number of pins, where K is an integer greater than 1; and

a pattern memory for storing the input signal patterns and the output signal patterns.

2. A test system according to claim 1, wherein each control unit is a multiplexer having K number of inputs.

3. A test system according to claim 1, wherein each control unit is configured to receive the control signal via a data bus.

4. A test system according to claim 1, wherein the pins of each pin group are output pins, wherein the pattern memory includes an input pattern memory for storing input signal patterns and an output pattern memory for storing output signal patterns, and wherein the output pattern memory stores output signal patterns from an external device according to a state of the control signal.

5. A test system according to claim 1, wherein the pins of each pin group are input pins, wherein the pattern memory includes an input pattern memory for storing input signal patterns and an output pattern memory for storing predicted

output signal patterns, and wherein the input pattern memory stores input signal patterns from an external device according to a state of the control signal.

6. A test system according to claim 1, wherein the pins of each pin group include input pins and/or output pins, wherein the pattern memory includes an input pattern memory for storing input signal patterns and an output pattern memory for storing predicted output signal patterns, wherein the input pattern memory stores the input signal patterns from an external device according to a state of the control signal, and wherein the output pattern memory stores the output signal patterns from the external device according to a state of the control signal.

7. A test system according to claim 1, wherein the pins of each pin group are output pins, wherein the pattern memory includes an input pattern memory for storing the input signal patterns and an output pattern memory for storing predicted output signal patterns, and wherein the predicted output signal patterns are stored in a buffer memory and loaded into the output pattern memory as occasion demands.

8. A method of testing a semiconductor device, the method comprising:

selecting pins from among a plurality of pins of the semiconductor device;

dividing the selected pins into a plurality of pin groups, each pin group comprising a desired plural number of pins;

generating a control signal;

electrically connecting a comparator and driver unit to a pin in a corresponding one of the pin groups of the semiconductor device according to the control signal;

applying input signal patterns from an input pattern memory to input pins of the semiconductor device; and

comparing data output from output pins of the semiconductor device with output signal patterns output from an output pattern memory.

9. A method according to claim 8, wherein the selected pins are input pins of the semiconductor device, and wherein the input signal patterns are stored in the input pattern memory according to a state of the control signal.

10. A method according to claim 8, wherein the selected pins are output pins of the semiconductor device, and wherein the output signal patterns are stored in the output pattern memory according to a state of the control signal.

11. A method according to claim 8, wherein all of the pins of the semiconductor device are selected and divided into pin groups, wherein the input signal patterns are output from an external storage device and stored in the input pattern memory according to a state of the control signal, and wherein the output signal patterns are output from the external storage device and stored in the output pattern memory according to the state of the control signal.

12. A pattern memory for use in a semiconductor device test system, said pattern memory comprising:

an input pattern memory; and

an output pattern memory, wherein one or more signal patterns are loaded into the pattern memory based on a control signal.

13. A pattern memory according to claim 12, wherein output signal patterns are loaded into the output pattern memory based on the control signal.

14. A pattern memory according to claim 12, wherein input signal patterns are loaded into the input pattern memory based on the control signal.

15. A pattern memory according to claim 12, wherein input signal patterns are loaded into the input pattern memory and output signals are loaded into the output pattern memory based on the control signal.

16. A method of testing a semiconductor device having many pins using a test system having fewer pins, said method comprising:

selectively connecting a pin of the test system to a pin of the semiconductor device based on a control signal.

17. A method according to claim 16, wherein the pin of the test system comprises a comparator and driver unit, said comparator and driver unit comprising a comparator configured to compare an output pattern from an output pin of the semiconductor device with a predetermined output pattern and a driver configured to drive an input pattern for an input pin of the semiconductor device, and wherein the comparator and driver unit is selectively connected to the pin of the semiconductor device based on the control signal.

18. A method according to claim 16, wherein pins of the semiconductor device are divided into a plurality of pin groups, each pin group comprising a plurality of pins.

19. A method according to claim 18, wherein the pin of the test system is selectively connected to one of the pins in a corresponding pin group via a control unit based on the control signal.

20. A method according to claim 18, wherein the pin of the test system comprises a comparator and driver unit and a control unit and wherein the control unit selectively connects one of the pins from a corresponding pin group to the comparator and driver unit based on the control signal.